CLAIMS

1. A semiconductor device, comprising:

a test circuit;

a first element; and

a second element comprising at least one of a transmitter and a receiver; wherein when the first element is coupled to the test circuit and the second element is coupled to the first element, at least one of the first and second elements is capable of testing another one of the first and second elements using the test circuit; and

the first element comprises a transmitter when the second element comprises a receiver and the first element comprises a receiver when the second element comprises a transmitter.

2. The semiconductor device of claim 1, wherein the semiconductor device is configured to operate at high frequencies.

3. The semiconductor device of claim 1, wherein the semiconductor device is configured to operate at a frequency of at least 1 Gigahertz.

4. The semiconductor device of claim 1, wherein the semiconductor device is configured to operate at a frequency of at least 3 Gigahertz.

5. The semiconductor device of claim 1, wherein the test circuit includes a pattern generator and a pattern compare circuitry.

6. The semiconductor device of claim 1, wherein the semiconductor device is configured to be coupled to at least one reference signal that includes a voltage reference signal, V_{REF}, and wherein the test circuit includes at least one

comparator circuit for comparing at least one voltage signal representing received data with the V_{REF} signal.

7. The semiconductor device of claim 6, wherein the at least one reference signal further includes a time reference signal, T_{REF}, and the high bandwidth test circuit includes at least one analog sampling circuit controlled by the T_{REF} signal, wherein the analog sampling circuit receives at least one voltage signal representing received data, such that T_{REF} determines a time offset between receipt of the at least one voltage signal by the receiver and evaluation of the voltage signal by the receiver.

8. The semiconductor device of claim 7, wherein the T_{REF} signal is scannable so as to characterize an actual output eye of the transmitter.

9. The semiconductor device of claim 7, wherein the T_{REF} signal is scannable so as to characterize an actual input eye of the receiver.

10. The semiconductor device of claim 1, wherein the semiconductor device is coupled to an interconnect to receive and transmit a complementary voltage value V_N and a true voltage value V_P, wherein the test circuit further comprises:

a test pattern generation circuit that generates test patterns for transmission to a component under test;

a test pattern comparison circuit that compares a generated test pattern with a pattern received from a component under test;

a first differential comparator that compares V_N with a voltage reference value, V_{REF} to produce a first result;

a second differential comparator that compares V_P with a voltage reference value, V_{REF} to produce a second result; and

a multiplexer that selects one of the first result and the second result to transmit to the comparator for comparison with the test pattern.

11. The semiconductor device of claim 10, wherein the test circuit further comprises an analog sampling circuit that delays the V_P and V_N signals under control of a T_{REF} signal so as to decouple parameters of the transmitter and the receiver.

12. The semiconductor device of claim 11, wherein the delayed V_P and V_N signals produce a third result, and wherein the multiplexer further selects one of the first result, the second result, and the third result to transmit to the comparator for comparison with the test pattern.

13. The semiconductor device of claim 12, wherein the transmitter is coupled to the receiver via an interconnect, and wherein the transmitter and the receiver are on a semiconductor wafer.

14. The semiconductor device of claim 12, wherein the transmitter is coupled to the receiver via an interconnect, wherein the interconnect is in a system and is used for system communication between the transmitter and the receiver.

15. A semiconductor circuit component coupleable to an external receiver and an external transmitter, the semiconductor component comprising:

a first transmitter coupled to a first signal path and configurable to drive a first signal according to predetermined transmitter specification parameters; and

a first receiver coupled to a second signal path and configurable to sample a second signal according to predetermined receiver specification parameters, wherein,

when the component is configured to operate in a first mode, the first signal path is coupled to the external receiver, and the second signal path is coupled to the external transmitter, and

when the component is further configurable to operate in a second mode in which,

the first signal path is coupled to the second signal path;

the first receiver is operable to evaluate the first signal for compliance with the predetermined transmitter specification parameters; and

the first transmitter is operable to evaluate the second signal for compliance with the predetermined receiver specification parameters.

16. The component of claim 15, wherein the component is configured to operate at high frequencies.

17. The component of claim 16, wherein the semiconductor device is configured to operate at a frequency of at least 1 Gigahertz.

18. The component of claim 16, wherein the semiconductor device is configured to operate at a frequency of at least 3 Gigahertz.

19. The component of claim 15, wherein the predetermined transmitter specifications of the first transmitter and the predetermined receiver specification parameters of the first receiver must be met for the first transmitter and the first receiver to be suitable for operation in the first mode, and wherein evaluation comprises determining that the first transmitter and the first receiver operate properly when the respective predetermined specification parameters are met.

20. The component of claim 15, wherein the predetermined transmitter specification parameters of the first transmitter and the predetermined receiver

specification parameters of the first receiver must be met for the first transmitter and the first receiver to be suitable for operation in the first mode, and wherein evaluation comprises:

determining an amount of margin present between operating characteristics of the first transmitter and the predetermined transmitter specification parameters being evaluated; and

determining an amount of margin present between operating characteristics of the first receiver and the predetermined receiver specification parameters being evaluated.

21. The component of claim 15, wherein, in the second mode, the first transmitter and the first receiver are in different interface blocks in the component and are each configurable to be coupled via an external interconnect.

22. The component of claim 15, wherein, in the second mode, the first transmitter and the first receiver are in a same interface block in the component and are coupled via an internal interconnect.

23. The component of claim 15, further comprising a first timing circuit that receives a first external timing signal and produces a first internal timing signal.

24. The component of claim 23, wherein the first internal timing signal is coupled to the first transmitter, and an internal timing event on the first internal timing signal causes the first transmitter to drive a first symbol on the first signal.

25. The component of claim 23, wherein the first internal timing signal is coupled to the first receiver, and an internal timing event on the first internal

timing signal causes the first receiver to sample a first symbol on the second signal.

26. The component of claim 23, wherein the first timing circuit aligns an internal timing event on the internal timing signal with an external timing event on the external timing signal.

27. The component of claim 23, wherein the first timing circuit creates at least two internal timing events on the first internal timing signal, that are each associated with an external timing event on the external timing signal.

28. The component of claim 23, wherein the first timing circuit creates an internal timing event on the internal timing signal, wherein the internal timing event has a fixed time offset relative to an external timing event on an associated external timing signal.

29. The component of claim 23, wherein the first timing circuit creates an internal timing event on the internal timing signal, wherein the internal timing event has an adjustable time offset relative to an external timing event on the associated external timing signal.

30. The component of claim 29, wherein the adjustable time offset is specified by a value held in a register in the component.

31. The component of claim 29, wherein evaluation of the respective predetermined specification parameters of the receiver and the transmitter includes accessing a value that determines the adjustable time offset.

32. The component of claim 23, wherein evaluation of the respective predetermined specification parameters of the receiver and the transmitter includes measuring a position of an external timing event on the first external timing signal.

33. The component of claim 15, further comprising:

a first timing circuit that receives a first external timing signal and produces a first internal timing signal; and

a second timing circuit that receives the second external timing signal and produces a second internal timing signal, such that the first internal timing signal is coupled to the first transmitter, and the second internal timing signal is coupled to the first receiver, so that a first timing event on the first internal timing signal causes the first transmitter to drive a first symbol on the first signal and a second timing event on the second internal timing signal causes the first receiver to sample a second symbol on the second signal.

34. The component of claim 33, wherein evaluation of the specification parameters of the receiver and the transmitter comprises:

measuring a position of a first external timing event on the first external timing signal; and

measuring a position of a second external timing event on the second external timing signal, wherein the first external timing event is associated with the first internal timing event and the second external timing event is associated with the second internal timing event.

35. The component of claim 34, wherein the first external timing event is aligned with the first internal timing event and the second external timing event is aligned with the second internal timing event

36. The component of claim 15, further comprising:

a first timing circuit that receives a first external timing signal and produces a first internal timing signal; and

a second timing circuit that receives the first external timing signal and produces a second internal timing signal, such that the first internal timing signal is coupled to the first transmitter, and the second internal timing signal is coupled to the first receiver, so that a first timing event on the first internal timing signal causes the first transmitter to drive a first symbol on the first signal and a second timing event on the second internal timing signal causes the first receiver to sample a second symbol on the second signal.

37. The component of claim 36, wherein:

the first timing circuit creates a first internal timing event on the first internal timing signal;

the first internal timing event has a first adjustable time offset relative to a first external timing event on the associated external timing signal;

wherein the second timing circuit creates a second internal timing event on the second internal timing signal; and

wherein the second internal timing event has a second adjustable time offset relative to a second external timing event on the associated external timing signal.

38. The component of claim 37, wherein the first adjustable time offset is specified by a first value held in a first register in the component and the second adjustable time offset is specified by a second value held in a second register in the component.

39. The component of claim 37, wherein evaluation of the respective predetermined specification parameters of the receiver and the transmitter

includes accessing a first value that determines the first adjustable time offset and includes accessing a second value that determines the second adjustable time offset.

40. The component of claim 15, wherein a voltage discriminator circuit is coupled to one of the first signal and the second signal, and measures a voltage level of one of the first signal and the second signal in the course of evaluating the respective predetermined transmitter and receiver specification parameters.

41. The component of claim 40, wherein a voltage reference signal is coupled to the voltage discriminator circuit to provide a voltage comparison standard for measuring a voltage level on one of the first signal and the second signal.

42. The component of claim 41, wherein measuring includes at least one comparison of a voltage level of one of the first signal and the second signal and a voltage reference signal

43. The component of claim 41, wherein the voltage discriminator circuit is a differential comparator with one input coupled to one of the first signal and the second signal and another input coupled to the voltage reference signal.

44. The component of claim 41, wherein the voltage reference signal is configurable to be generated outside the component.

45. The component of claim 41, wherein the voltage reference signal is generated inside the component by a voltage reference generator circuit, and

wherein the voltage reference generator circuit is coupled to a register containing a value that adjusts a voltage level of the voltage reference signal.

46. The component of claim 15, wherein the receiver includes a voltage discriminator circuit and measures a voltage level of the second signal in the course of evaluating the respective predetermined transmitter and receiver specification parameters.

47. The component of claim 46, wherein a voltage reference signal is coupled to the voltage discriminator circuit to provide a voltage comparison standard for measuring a voltage level on the second signal.

48. The component of claim 47, wherein measuring includes at least one comparison of a voltage level of the second signal and the voltage reference signal.

49. The component of claim 47, wherein the voltage discriminator circuit is a differential comparator with one input coupled to the second signal and another input coupled to the voltage reference signal.

50. The component of claim 47, wherein the voltage reference signal is configurable to be generated outside the component.

51. The component of claim 47, wherein the voltage reference signal is generated inside the component by a voltage reference generator circuit, wherein the voltage reference generator circuit is coupled to a register containing a value that adjusts a voltage level of the voltage reference signal.

52. The component of claim 15, wherein a timing discriminator circuit couples a third signal to one of the first signal and the second signal, wherein the third signal is further coupled to a third receiver on the component, wherein the third receiver being similar to the first receiver, and wherein the time discriminator circuit is used to evaluate the respective predetermined specification parameters of the first transmitter and of the first receiver.

53. The component of claim 52, wherein a timing reference signal is coupled to the timing discriminator circuit, and wherein the timing reference signal is configurable to be generated outside the component.

54. The component of claim 53, wherein a timing event on the timing reference signal causes the third signal to assume a same value as the one of the first signal and second signal.

55. The component of claim 53, wherein a timing event on the timing reference signal causes the third signal to become independent of the one of the first signal and second signal, and to retain a value as of the timing event.

56. The component of claim 53, wherein the timing discriminator circuit includes an MOS pass transistor coupling the one of the first signal and second signal and the third signal, wherein the timing reference signal is coupled to the gate of the MOS pass transistor, and wherein a capacitor is coupled between the third signal and a fixed voltage reference.

57. The component of claim 53, wherein the timing reference signal is coupled directly from an external source to the timing discriminator circuit with an internal interconnect.

58. The component of claim 52, wherein a timing reference signal is coupled to the timing discriminator circuit and is generated inside the component by a timing reference generator circuit, to which is coupled a register containing a value which adjusts the timing offset of a timing event on the timing reference signal.

59. The component of claim 15, wherein a first timing discriminator circuit couples a third signal to the second signal, and a second timing discriminator circuit couples the third signal to a fourth signal, wherein the fourth signal is coupled to a third receiver on the component, the third receiver being similar to the first receiver, wherein the first and second time discriminator circuits are used to evaluate the respective predetermined specification parameters of the first transmitter and of the first receiver.

60. The component of claim 15, wherein the first receiver consists of a first timing discriminator circuit coupled to one of a voltage discriminator circuit and a second timing discriminator circuit, such that the in the first mode of operation the first timing discriminator couples the second signal to the one of a voltage discriminator circuit and a second timing discriminator circuit, and in the second mode of operation, the first time discriminator circuit is used to evaluate the respective predetermined specification parameters of the first transmitter and of the first receiver.

61. The component of claim 60, wherein a timing reference signal is coupled to the first timing discriminator circuit and is configurable to be generated outside the component, and wherein the timing reference signal is coupled directly from an external source to the timing discriminator circuit with an internal interconnect.

62. The component of claim 15, further comprising a current control circuit coupled to the transmitter, wherein the current control circuit determines a current passing through the first transmitter to determine a voltage level driven on the first signal in the first mode and in the second mode.

63. The component of claim 62, further comprising a current reference signal coupled to the current control circuit to provide a current comparison standard for determining a current passing through the first transmitter.

64. The component of claim 63, wherein the current control circuit and the first transmitter each include a plurality of transistor elements whose conductive strengths form a binary sequence.

65. The component of claim 63, wherein the current reference signal is configurable to be generated outside the component.

66. The component of claim 63, further comprising:

a current reference generator circuit that generates the current reference signal inside the component; and

a register coupled to the reference generator circuit, wherein the register stores a value that adjusts a value of the current reference signal.

67. The component of claim 63, wherein the current reference signal is varied between at least two values during evaluation of the transmitter and receiver specification parameters in the second mode.

68. The component of claim 15, further comprising:

a termination control circuit;

a termination element coupled to the termination control circuit and to one of the first signal and the second signal, wherein the termination control circuit determines a value of a termination load present on one of the first signal and the second signal in the second mode, and in the first mode.

69. The component of claim 68, further comprising a termination reference signal coupled to the termination control circuit to provide a termination comparison standard for determining a value of a termination load present on one of the first signal and the second signal.

70. The component of claim 69, wherein the termination control circuit and the termination element each include a plurality of transistor elements whose conductive strengths form a binary sequence.

71. The component of claim 69, wherein the termination reference signal is configurable to be generated outside the component.

72. The component of claim 69, further comprising:

a termination reference generator circuit that generates the termination reference signal inside the component; and

a register coupled to the termination generator circuit, wherein the register stores a value that adjusts a value of the termination reference signal.

73. The component of claim 69, wherein the termination reference signal is varied between at least two values in the second mode.

74. The component of claim 73, wherein the termination voltage signal is varied between at least two values in the second mode.

75. The component of claim 15, further comprising a termination element coupled to a termination voltage signal, and further coupled to one of the first signal and the second signal, wherein the termination element determines voltage levels present on one of the first signal and the second signal in the second mode and in the first mode.

76. The component of claim 75, wherein the termination voltage signal is configurable to be generated outside the component.

77. The component of claim 75, further comprising:

a termination voltage generator circuit that generates the termination voltage signal inside the component; and

a register coupled to the termination voltage generator circuit, wherein the register stores a value that adjusts a value of the termination voltage signal.

78. The component of claim 15, further comprising at least one pattern generator circuit, wherein pattern data from the at least one pattern generator circuit is coupled to the first transmitter to be driven as transmitter pattern data on the first signal, and to be sampled by the receiver as received pattern data on the second signal.

79. The component of claim 15, further comprising at least one pattern comparison circuit that compares the received pattern data to the transmitted pattern data.

80. The component of claim 15, wherein at least one of the first signal and the second signal are encoded using two differential voltage values.

81. The component of claim 15, wherein at least one of the first signal and the second signal are encoded using single-ended voltage values.

82. The component of claim 15, wherein at least one of the first signal and the second signal are encoded using single-ended voltage values with reference to an external reference voltage value.

83. The component of claim 15, wherein at least one of the first signal and the second signal are each bidirectional.

84. The component of claim 15, wherein at least one of the first signal and the second signal are each unidirectional.

85. The component of claim 15, wherein the first transmitter includes at least one unipolar driver.

86. The component of claim 15, wherein the first transmitter includes at least one bipolar driver.

87. The component of claim 15, wherein the first transmitter uses an external reference value to generate signal values.

88. The component of claim 15, further comprising at least one calibration circuit, wherein the first transmitter uses an external reference value and the at least one calibration circuit to generate signal values.

89. The component of claim 88, wherein the calibration circuitry is adjustable.

90. The component of claim 89, wherein the calibration circuitry is adjustable using a value in a register of the component.

91. The component of claim 15, wherein at least one of the first signal and the second signal is coupleable to an interconnect that couples the component to one other component.

92. The component of claim 15, wherein at least one of the first signal and the second signal is coupleable to an interconnect that couples the component to at least two other components.

93. The component of claim 15, wherein at least one of the first signal and the second signal use current-mode operation.

94. The component of claim 15, wherein at least one of the first signal and the second signal use voltage-mode operation.

95. The component of claim 15, further comprising at least one slew rate control circuit coupled to control respective slew rates of at least one of the first signal and the second signal.

96. The component of claim 15, wherein at least one of the first signal and the second signal is coupled to respective external termination loads.

97. The component of claim 15, wherein at least one of the first signal and the second signal is coupled to respective internal termination loads.

98. The component of claim 97, wherein at least one of the internal termination loads is calibrated to an external reference value.

99. The component of claim 98, wherein at least one of the internal termination loads is adjustable.

100. The component of claim 99, wherein at least one of the internal termination loads is adjusted using a value in an internal register.

101. An electronic system comprising:

at least one semiconductor component configurable to perform testing functions, wherein the at least one semiconductor component has at least two operational modes comprising a normal mode and a test mode, the at least one semiconductor component comprising,

a transmitter;

a receiver; and

a test circuit, wherein in the test mode the transmitter is configurable to test the receiver and the receiver is configured to test the transmitter.

102. The system of claim 101, wherein in at least one semiconductor component is a component configured to operate at high frequencies.

103. The system of claim 102, wherein the semiconductor component is configured to operate at a frequency of at least 1 Gigahertz.

104. The system of claim 102, wherein the semiconductor component is configured to operate at a frequency of at least 3 Gigahertz.

105. The system of claim 101, wherein in the test mode, the transmitter and the receiver are on a same semiconductor component.

106. The system of claim 101, wherein in the test mode, the transmitter and the receiver are on different interfaces of a same semiconductor component.

107. The system of claim 101, wherein in the test mode, the transmitter and the receiver are on different semiconductor components.

108. The system of claim 101, wherein the at least one semiconductor component comprises a memory interface on a memory component and a memory controller interface on a memory controller component, and wherein the memory component and the memory controller component are coupled via an interconnect in the test mode and in the normal mode.

109. The system of claim 108, wherein the interconnect is a high frequency interconnect.

110. The system of claim 108, wherein the interconnect is configured to operate at a frequency of at least 1 Gigahertz.

111. The system of claim 108, wherein the interconnect is configured to operate at a frequency of at least 3 Gigahertz.

112. The system of claim 101, wherein the at least one semiconductor component is coupled to a plurality of reference signals, including a voltage reference signal, V_{REF}, a receiver clock reference signal, CLK_{RREF}, a transmitter clock reference signal CLK_{TREF}, and a current reference signal, I_{REF}, and wherein the reference signals are scanned in the test mode, wherein scanning comprises sweeping a value of a reference signal to determine an event on another signal.

113. The system of claim 112, wherein a differential comparator receives the V_{REF} signal and compares the V_{REF} signal to a signal voltage on the interconnect as the V_{REF} signal is scanned to produce a test output signal.

114. The system of claim 112, wherein the plurality of reference signals further comprise a time reference signal, T_{REF}, and wherein the test circuit further comprises an analog sampling circuit controlled by the T_{REF} signal so as to control sampling times of a signal voltage on the interconnect in the test mode independent of individual interface parameters, wherein the analog sampling circuit produces a time test voltage signal.

115. The system of claim 114, wherein the test circuit further comprises:

a test pattern circuit;

a register that holds the test output signal and the time test voltage signal; and

a selection circuit coupled to the test pattern circuit, that selects a value from the register to be compared to a test pattern.

116. The system of claim 112, wherein the plurality of reference signals further comprise a test current reference signal $I_{TL\text{-}REF}$ that controls a test current generated to allow a pin of one of the at least one semiconductor components to test itself.

117. An electronic system comprising:

at least one semiconductor component configurable to perform testing functions, wherein the at least one semiconductor component has at least two operational modes comprising a normal mode and a test mode, the at least one semiconductor component comprising,

a transmitter;

a receiver; and

a test circuit, wherein in the test mode the transmitter is configurable to test the receiver or the receiver is configured to test the transmitter.

118. A method for a semiconductor component to be tested by another semiconductor component, the method comprising:

generating a test pattern;

storing the test pattern in the semiconductor component;

providing a reference signal to the semiconductor component;

generating an operational signal by processing a data signal in the semiconductor component;

scanning the reference signal;

comparing the operational signal to the reference signal, while scanning the reference signal ; and

comparing a result of the comparison with the test pattern.

119. The method of claim 118, wherein at least one of the semiconductor component and the other semiconductor component is configured for operation at high frequencies.

120. The method of claim 119, wherein at least one of the semiconductor component and the other semiconductor component is configured for operation at a frequency of at least 1 Gigahertz.

121. The method of claim 119, wherein at least one of the semiconductor component and the other semiconductor component is configured for operation at a frequency of at least 3 Gigahertz.

122. The method of claim 118, wherein the method is performed by the semiconductor component on the other semiconductor component, and wherein the semiconductor component and the other semiconductor component are on at least one semiconductor wafer.

123. The method of claim 122, wherein the semiconductor component and the other semiconductor component comprise a transmitter and a receiver, and wherein the plurality of signals further comprises a time reference signal that decouples semiconductor component transmitter timing parameters from semiconductor component receiver timing parameter, the method further comprising scanning the time reference signal to define a output eye region for the transmitter, including:

creating a series of timing events, including an active clock edge that causes the transmitter to output data;

determining a time after an active clock edge when the output data becomes valid; and

determining a time after an active clock edge when the output data becomes invalid.

124. The method of claim 123, further comprising using the time reference signal to control an analog sampler that samples the output data and creates a time offset between when the output data becomes valid and when the output data is sampled as input data by the receiver.

125. The method of claim 124, further comprising:

setting the time offset using the time reference signal such that an input eye region of the receiver occurs within the output eye region defined for the transmitter; and

scanning a receiver clock signal to determine whether a setup time specification and a hold time specification for the receiver are met.

126. The method of claim 118, wherein the method is performed by the semiconductor component on the other semiconductor component, and wherein the semiconductor component and the other semiconductor component are in at least one component package.

127. The method of claim 126, wherein the method is performed on the high-speed receiver circuit, the method comprising:

scanning a voltage reference signal; and

comparing the scanned voltage reference signal with a normal operational signal of the receiver to determine a high input voltage and a low input voltage.

128. The method of claim 127, further comprising scanning a transmitter clock reference signal to determine whether a setup time specification and a hold time specification for the transmitter are met.

129. The method of claim 118, wherein the semiconductor component and the other semiconductor component comprises a high frequency transmitter circuit and a high frequency receiver circuit.

130. The method of claim 129, wherein the high frequency transmitter circuit and the high frequency receiver circuit operate at a frequency of at least 1 Gigahertz.

131. The method of claim 129, wherein the high frequency transmitter circuit and the high frequency receiver circuit operate at a frequency of at least 3 Gigahertz.

132. The method of claim 129, wherein the method is performed on the high-speed transmitter circuit, the method further comprising:

scanning a voltage reference signal and;

comparing the scanned voltage reference signal with a normal operational signal of the transmitter to determine a high output voltage and a low output voltage.

133. The method of claim 132, further comprising scanning a receiver clock reference signal to determine whether a setup time specification and a hold time specification for the receiver are met.

134. A method for using one component to test and characterize another component, comprising:

receiving at least one first signal having a first frequency;

receiving a plurality of second reference signals having a plurality of second frequencies, wherein at least one of the second frequencies is lower than the first frequency;

generating and storing a test pattern;

scanning one of the second reference signals;

comparing an operational signal to one of the second reference signals, while scanning one of the reference signals, wherein the operational single comprises a data signal processed by a circuit during operation; and

comparing a result of the comparison with the test pattern.

135. A semiconductor circuit component comprising:

a transmit interface comprising,

a first transmitter; and

transmitter test circuitry; and

a receive interface comprising,

a first receiver: and

receiver test circuitry, wherein the first transmitter drives a first signal according to predetermined transmitter specifications, the first receiver samples a second signal according to predetermined receiver specifications, and wherein the component is configurable to operate in a test mode in which,

the first signal is coupled to the second signal such that the first receiver evaluates transmitter specification parameters of the first transmitter; and

the first signal is coupled to the second signal such that the first transmitter evaluates receiver specification parameters of the first receiver.

136. The component of claim 135, wherein the receive interface and the transmit interface are each configured to transfer data at rates equal to or greater than 3GHz.

137. The component of claim 135, wherein the transmitter test circuitry comprises a first pattern source element, and wherein a first pattern set transmitted from the first pattern source element to the first transmitter, and is driven by the first transmitter onto the first signal during operation in the test mode.

138. The component of claim 137, wherein the transmitter test circuitry further comprises a first pattern storage element coupled to the first pattern source element, wherein the first pattern storage element stores the first pattern set as the first pattern set is generated.

139. The component of claim 137 in which the first pattern set is generated by circuitry in the first pattern source element.

140. The component of claim 137 in which the first pattern set is generated by circuitry external to the component and communicated to the first pattern source element.

141. The component of claim 137 in which the first pattern set is generated when the first pattern source element is controlled by at least one first external sideband signal whose transfer rate is lower than that of the first signal.

142. The component of claim 137, wherein the receiver test circuitry comprises:

a delay element coupled to the first pattern source element; and

a compare element coupled to the delay element, wherein the first receiver samples a second pattern set on the second signal, the first pattern set is delayed by the first delay element to form a third pattern set, and wherein the compare element is compares the first pattern set to the third pattern set.

143. The component of claim 137, wherein the transmitter test circuitry further comprises a memory array coupled to the first pattern source element, wherein the first pattern set is stored in the memory array.

144. The component of claim 143, wherein at least one pattern set is written from the first pattern source element to the memory array.

145. The component of claim 143, wherein at least one pattern set is read from the memory array to the first transmitter and driven onto the first signal during operation in the test mode.

146. The component of claim 143, wherein the receiver test circuitry further comprises:

a delay element coupled to the memory array; and

a compare element coupled to the delay element, wherein the first receiver samples a second pattern set on the second signal such that the first pattern set is delayed by the delay element to form a third pattern set, and wherein the compare element compares the first pattern set to the third pattern set.

147. The component of claim 135, further comprising a first pattern source element, wherein the first receiver samples a first pattern set on the second signal, and a second pattern set is provided by the first pattern source element during operation in the test mode.

148. The component of claim 147, wherein the first pattern source element includes a first pattern storage element used to accumulate the first pattern set as the first pattern is generated.

149. The component of claim 147, wherein the first pattern set is generated by circuitry in the pattern source element.

150. The component of claim 147, wherein the first pattern set is generated by circuitry external to the component and is communicated to the pattern source element.

151. The component of claim 147, wherein the first pattern set is generated when the pattern source element is controlled by at least one first external sideband signal whose transfer rate is lower than that of the second signal.

152. The component of claim 147, further comprising a compare element coupled to the first receiver and the first pattern source element, wherein the compare element compares the first pattern set to the second pattern set.

153. The component of claim 147, further comprising a memory array coupled to the first pattern source element, wherein the second pattern set resides in the memory array.

154. The component of claim 153, wherein at least one pattern set is written from the first pattern source element to the memory array.

155. The component of claim 153, wherein at least one pattern set is read from the memory array.

156. The component of claim 153, further comprising a compare element coupled to the first receiver and the memory array, wherein the compare element compares the first pattern set to the second pattern set.

157. An electronic system comprising:

a first component comprising a first transmitter configured to drive a first signal onto a first external interconnect according to a set of transmitter specification parameters; and

a second component comprising a first receiver configured to sample the first signal from the first external interconnect according a set of receiver specification parameters, wherein,

the first component and the second component are configurable to operate in a normal mode in which the first signal is configurable to be driven by the first component and sampled by the first receiver;

the first component and the second component are further

configurable to operate in a first test mode in which the first receiver evaluates the transmitter specification parameters of the first transmitter; and

the first component and the second component are further configurable to operate in a second test mode in which first transmitter evaluates the receiver specification parameters of the first receiver.

158. The system of claim 157, wherein the first component and the second component are each semiconductor components configured to operate at frequencies of 1 GHz or greater.

159. The system of claim 157, wherein the first component and the second component are each semiconductor components configured to operate at frequencies of 3 GHz or greater.

160. The system of claim 157, wherein system evaluation of the first component is performed in the first test mode.

161. The system of claim 157, wherein system evaluation of the second component is performed in the second test mode.

162. The system of claim 157, wherein the first component further comprises a second receiver coupled with a second interconnect to the first transmitter, wherein the first component is further configurable to operate in a third test mode in which the second receiver evaluates the transmitter specification parameters of the first transmitter.

163. The system of claim 162, wherein the second interconnect is an internal interconnect of the first component.

164. The system of claim 162, wherein the second interconnect is an interconnect external to the first component.

165. The system of claim 162, wherein wafer evaluation of the first component is performed in the third test mode.

166. The system of claim 162, wherein package evaluation of the first component is performed in the third test mode.

167. The system of claim 157, wherein the second component further comprises a second transmitter coupled with a second interconnect to the first receiver, wherein the second component is further configurable to operate in a third test mode in which the second transmitter evaluates the receiver specification parameters of the first receiver.

168. The system of claim 167, the second interconnect is an internal interconnect of the second component.

169. The system of claim 167, wherein the second interconnect is external to the second component.

170. The system of claim 167, wherein wafer evaluation of the second component is performed in the third test mode.

171. The system of claim 167, wherein package evaluation of the second component is performed in the third test mode.

172. The system of claim 157, further comprising at least one third component coupled to the external interconnect, wherein the first component is

further configurable to operate in a third test mode in which the first transmitter is coupled with a second external interconnect to a second receiver on the third component, so that the second receiver evaluates the transmitter specification parameters of the first transmitter.

173. The system of claim 172, wherein wafer evaluation of the first component is performed in the third test mode.

174. The system of claim 172, wherein package evaluation of the first component is performed in the third test mode.

175. The system of claim 172, wherein the third component is substantially the same as the first component.

176. The system of claim 157, further comprising at least one third component coupled to the external interconnect, wherein the second component is further configurable to operate in a third test mode in which the first receiver is coupled with a second external interconnect to a second transmitter on the third component, so that the second transmitter evaluates the receiver specification parameters of the first receiver.

177. The system of claim 176, wherein wafer evaluation of the second component is performed in the third test mode.

178. The system of claim 176, wherein package evaluation of the second component is performed in the third test mode.

179. The system of claim of claim 176, wherein the third component is substantially similar to the second component.

180. A device, comprising:

a test circuit;

a first element, coupled to the test circuit, including

a transmitter;

a second element, coupled to the first element and the test circuit, including a receiver; and

means for testing the first element using the second element and the test circuit.

181. A device, comprising:

a test circuit;

a first element, coupled to the test circuit, including

a transmitter;

a second element, coupled to the first element and the test circuit, including a receiver; and

means for testing the second element using the first element and the test circuit.